Amendments to the Claims:

The listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1 – 42 (cancelled)

Claim 43. (previously presented) A programmable controller for use with a monitoring device, said programmable controller including:

at least one digital input interface,

at least one digital output interface for receiving data from at least one output register,

programmable logic hardware including a plurality of logic elements including flip-flops, and electrically configurable interconnections, said interconnections configurable to interconnect the logic elements as a logic processing circuit, said logic processing circuit arranged to implement a user control program defined by a user as a user control program circuit, said logic processing circuit configurable in said programmable logic hardware, and connected to said at least one digital input interface and said at least one digital output interface,

program loading circuits for configuring said programmable logic hardware with said logic processing circuit prior to initiating control, and where said programmable logic hardware, configured with the logic processing circuit, includes:

a plurality of logic processing circuit flip-flops for storing state data, and for each of these flip-flops, an associated support circuit, the support circuits arranged to operate selectively between first and second conditions, wherein in said first condition the support circuits cause the flip-flops to act as a shift register for transporting state data into and out of the logic processing circuit, and wherein in the second condition the support circuits cause the flip-flops to act as logic elements of said user control program, the support circuits being selected to operate in only one of either the first condition or the second condition at any one time, and

a monitoring services and control unit arranged to control and operate said logic processing circuit including:

a continuously cycling logic processing scan at least including said support circuits in both said first condition and said second condition, and when in said first condition said support circuits are arranged to operate to shift state data out of and into said logic processing circuit to provide read and write access to said plurality of logic processing flip-flops; and when in said second condition said programmable controller is arranged to operate to apply user clock pulses to said logic processing circuit and to update said at least one output register,

wherein said monitoring services and control unit is further arranged to perform a program swap operation, including circuits arranged to:

configure into an incoming section of programmable logic hardware an incoming logic processing circuit including an incoming user control program circuit,

terminate the continuously repeating logic processing circuit scan of an outgoing logic processing circuit and maintain the value stored in said at least one output register,

ensure the output data in the said at least one output register remains unchanged from the output data last stored from the user control program circuit when said support circuits were operated according to said second condition,

read the state data from said outgoing user control program circuit,

write the state data from said outgoing user control program circuit into the corresponding incoming state data storage units so that each state data bit in said incoming user program circuit that has a corresponding bit in said outgoing user control program circuit has its state set to the same state that existed in the corresponding bit in said outgoing user control program circuit, said write the state data including relocating, as necessary, state data bits at different addresses in said incoming section as compared to the addresses in said outgoing section from which they were read, and

start the continuously repeating logic processing circuit scan of said incoming logic processing circuit, and enabling said at least one output register to be updated.

Claim 44. (previously presented) The programmable controller as claimed in claim 43 further including circuits arranged to facilitate relocation of user control program circuit state data from a logic processing circuit in said outgoing section into the user control program circuit in a logic processing circuit in said incoming section, and circuits arranged to facilitate including:

relocating address memory circuits arranged to provide the address of a first bit in a pair of corresponding bits as a function of the address of the second bit in the same pair of corresponding bits.

Claim 45. (currently amended) The programmable controller as claimed in claim 44, wherein said monitoring services and control unit is arranged to operate to perform a program swap, said programmable logic hardware arranged in separately configurable sections~~section~~, said sections including:

an outgoing section, said outgoing section having an outgoing logic processing circuit arranged to operate, prior to the program swap, in a continuously repeating logic processing circuit scan cycle, and

an incoming section, said incoming section being inoperative prior to the program swap.

Claim 46. (previously presented) The programmable controller as claimed in claim 45 further arranged to allow the continuance of circuit operation after the occurrence of a circuit operational failure of a type that does not cause permanent physical damage to said programmable controller, including:

at least three separately configurable blocks of programmable logic hardware, each said block being equivalent to one said outgoing section and one said incoming section, and performing in order the steps of:

operating each said block in parallel and in synchronism,

identifying circuit failures, by comparing on a clock-by-clock basis the operation of each said block against each other said block, and determining when at least one said block operates differently to the other said blocks,

reconfiguring each said block that has failed and pausing the non-failing said blocks thus preserving the value stored in said output registers,

transferring the state of the non-failing said blocks to the reconfigured said block(s), and

restarting said blocks by enabling logic processing in parallel and in synchronism and enabling said output registers to be updated.

Claim 47. (currently amended) A programmable controller for use with a monitoring device, said programmable controller including:

at least one digital input interface,

at least one digital output interface for receiving data from at least one output register,

programmable logic hardware including a plurality of logic elements including flip-flops, and electrically configurable interconnections, said interconnections configurable to interconnect the logic elements as a logic processing circuit, said logic processing circuit arranged to implement a user control program defined by a user as a user control program circuit, said logic processing circuit configurable in said programmable logic hardware, and connected to said at least one digital input interface and said at least one digital output interface,

program loading circuits for configuring said programmable logic hardware with said logic processing circuit prior to initiating control, and where said programmable logic hardware, configured with the logic processing circuit, includes:

a plurality of logic processing circuit flip-flops for storing state data, and for each of these flip-flops, an associated support circuit, the support circuits arranged to operate selectively between first and second conditions, wherein in said first condition the support circuits cause the flip-flops to act as a shift register for transporting state data into and out of the logic processing circuit, and wherein in the second condition the support circuits cause the flip-flops to act as logic elements of said user control program, the support circuits being selected to operate in only one of either the first condition or the second condition at any one time,

wherein said plurality of logic processing circuit flip-flops are interconnected to form a shift register by the programmable ~~device~~ configuration process, and a monitoring services and control unit arranged to control and operate said logic processing circuit including:

a continuously cycling logic processing scan at least including said support circuits in both said first condition and said second condition, and when in said first condition said support circuits are arranged to operate to shift state data out of and into said logic processing circuit to provide read and write access to said plurality of logic processing flip-flops; and when in said second condition said programmable controller is arranged to operate to apply user clock pulses to said logic processing circuit and to update said at least one output register,

wherein said monitoring services and control unit is further arranged to perform a program swap operation, including circuits arranged to:

configure into an incoming section of programmable logic hardware an incoming logic processing circuit including an incoming user control program circuit,

terminate the continuously repeating logic processing circuit scan of an outgoing logic processing circuit and maintain the value stored in said at least one output register,

ensure the output data in the said at least one output register remains unchanged from the output data last stored from the user control program circuit when said support circuits were operated according to said second condition,

read the state data from said outgoing user control program circuit,

write the state data from said outgoing user control program circuit into the corresponding incoming state data storage units so that each state data bit in said incoming user program circuit that has a corresponding bit in said outgoing user control program circuit has its state set to the same state that existed in the corresponding bit in said outgoing user control program circuit, said write the state data including relocating, as necessary, state data bits at different addresses in said incoming section as compared to the addresses in said outgoing section from which they were read, and

start the continuously repeating logic processing circuit scan of said incoming logic processing circuit, and enable said at least one output register to be updated.

Claim 48. (previously presented) The programmable controller as claimed in claim 47 further including circuits arranged to facilitate relocation of user control program circuit state data from a logic processing circuit in said outgoing section into the user control program circuit in a logic processing circuit in said incoming section, said circuits arranged to facilitate including:

relocation address memory circuits arranged to provide the address of a first bit in a pair of corresponding bits as a function of the address of the second bit in the same pair of corresponding bits.

Claim 49. (previously presented) The programmable controller as claimed in claim 48, wherein said monitoring services and control unit is arranged to operate to perform a program swap, said programmable logic hardware arranged in separately configurable sections, said sections including:

an outgoing section, said outgoing section having an outgoing logic processing circuit arranged to operate, prior to the program swap, in a continuously repeating logic processing circuit scan cycle, and

an incoming section, said incoming section being inoperative prior to the program swap.